Micro UART

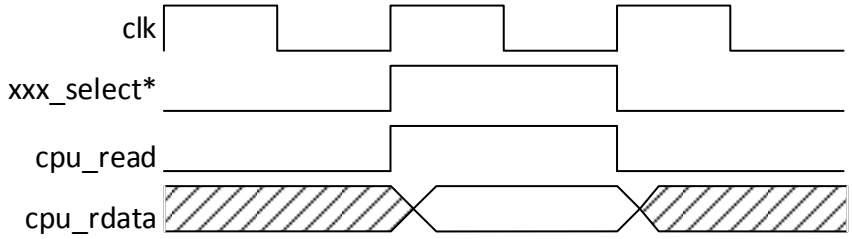
Free ware, 2015
Fen Logic Ltd.

Interface.

Hardware interface.

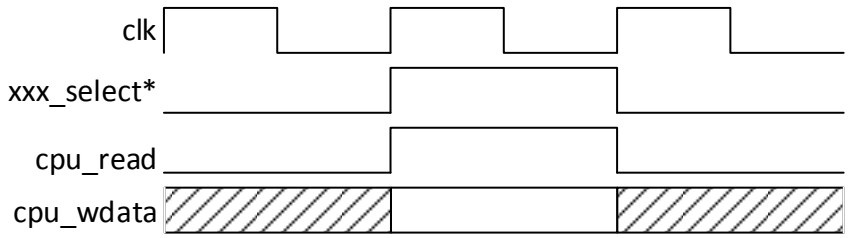
```
module micro_uart
(
   input              clk,            // system clock also used for baudrate
   input              reset_n,        // asynchronous active low reset

   // CPU bus
   input              data_select,    // High when cpu read/writes data reg.
   input              baud_select,    // High when cpu read/writes baud reg.
   input              cpu_read,       // High when cpu does read
   input              cpu_write,      // High when cpu does write
   input      [15:0]  cpu_wdata,      // Data written by cpu
   output reg [15:0]  cpu_rdata,      // Data back to cpu,
                                      //     0 when cpu_read is low

   //
   input              ser_in,         // Micro uart serial input
   output reg         ser_out         // Micro uart serial output
);
```

Read Cycle.



*The **data_select** or **baud_select** signals are optional. If neither is activated the status register is read.

Write Cycle.



*The **data_select** or **baud_select** signals are optional. If neither is activated the control register is written. (Except in the **mini_uart** which does not have a control register).

Control interface.

read	write	data_select	baud_select	operation
0	0	x	x	None
1	x	1	x	Read receive reg.
1	x	0	1	Read baud rate reg.
1	x	0	0	Read status
0	1	1	x	Write transmit reg.
0	1	0	1	Write baud rate reg.
0	1	x	x	Write control reg. (Only on micro_uart1 and higher)

APB interface.

psel	pwrite	address	operation
0	x	x	None
1	0	0	Read receive reg.
1	0	4	Read baud rate reg.
1	0	other	Read status
1	1	0	Write transmit reg.
1	1	4	Write baud rate reg.
1	1	other	Write control reg. (Only on micro_uart1 and higher)

Status register

Bit	Desciption	Version
15-5	Unused, always read as zero	
4	0 : Transmit interrupt pending 1 : No transmit interrupt pending This bit will be cleared when writing the data register or when disabling the transmit interrupts	1+
3	0 : Receive interrupt pending 1 : No receive interrupt pending This bit will be cleared when reading the data register or when disabling the receive interrupts	1+
2	0 : Transmitter busy 1 : Transmitter idle This bit will be cleared when writing the data register	All
1	0 : Receiver OK 1 : Input overflow detected This bit will be cleared when reading the data register	All
0	0 : Receive register is empty 1 : Receiver register has data This bit will be cleared when reading the data register	All

Control register

Note that only the micro_uart1 and higher revisions have a control register.

Bit	Desciption	Version
15-2	Unused, ignored on write	
1	0 : Transmit interrupt disabled 1 : Transmit interrupt enabled	1+
0	0 : Receive interrupt disabled 1 : Receive interrupt enabled	1+

Baud rate

The baud rate is set by writing the baud rate register. After a rest the register is set to zero but you can change that:

```
baud_count   <= 16'h0; // can set default baud rate here
```

To calculate the baud rate you must know the clock frequency (signal name = **`clk`**, revisions 1 and lower) or the reference clock frequency (signal name is **`ref_clock`**, for revisions 2 and higher). The micro UART uses eight times oversampling. The final baud rate is calculated using the following formula:

$$baud\ rate = \frac{clock\_freq}{(baudreg + 1) * 8}$$

Or to calculate the baud register value from the required baud rate:

$$baud\ reg = \frac{clock\_freq}{baud\_rate * 8} - 1$$

In the revisions < 3 the baud counter is re-loaded when it reaches zero. If the baud rate value is changed, it may make take up to 65535 clock cycles before the new value becomes active. In revision 3 and higher the baud rate counter is reloaded immediately after it is written.